REMARKS

Claims 1-22 stand rejected under § 102 on the basis of Tremblay et al. Remaining independent claims 1 and 22 have been amended to overcome this rejection, by reciting that all the pipelines have substantially the same instruction processing capability. Applicants traverse this rejection because Tremblay does not disclose (or suggest) this feature of the present invention.

Tremblay discloses a parallel-pipelined processor in which, if a pipeline generates a local stall, a global stall is generated which is conveyed to all the other pipelines of the processor in order to cause them to stall in cycles subsequent to that in which the local stall is generated.

It can be understood from Figure 2 of Tremblay and the discussion relating thereto in column 5, lines 43 to 58, that four pipelines are used to process instructions entered into the processor of Tremblay. Three of the pipelines are media functioning units (denoted by 220 in Figure 2) and the fourth is a general functioning unit (denoted by 222 in Figure 2). The media functioning units are multiple single-instruction multiple datapath (MSIMD) processors that operate synchronously, whereas the general functioning unit is a reduced instruction set (RISC) processor that is dedicated to the execution of specific parallel operations (as explained in column 5, lines 59 to 65). As stated in column 6, lines 40 to 43, a VLIW instruction word entered into the processor always includes one instruction that executes in the general functioning unit (GFU) and three instructions that are executed respectively in the three media functioning units (MFU). Thus, it would be clear to a skilled person that instructions entered into the processor of Tremblay are always organised into sub-

instruction packets such that one of these sub-instruction packets is fed to a dedicated pipeline (i.e. GFU) for specific processing. Notably, it would also be clear to the skilled person that extra processing power and/or circuitry would have to be used in Tremblay to split the instructions in the required manner and also to synchronise the release of the results of the GFU at the same time as the MFUs from the processor. The GFU cannot be taken as a supplementary unit to the parallel-pipelined processing architecture of the processor of Tremblay. Indeed, it is an integral part of it since some of the instructions entered into the processor are always routed through the GFU and processed thereby to be ultimately used in conjunction with the results of the MFUs in producing a final result.

Unlike the disclosure in Tremblay, no distinction is made between the processing capability of the multiple pipelines used in the processor of the present invention, as described in the specification of the present application. It would be clear to a skilled person consulting the specification (specifically, page 3, lines 15 to 20) that each of the pipelines is capable of multiple data, multi-path processing and has substantially the same configuration as the other pipelines in the processor. Unlike Tremblay, the present invention does not have a dedicated pipeline for processing specific data and, therefore, does not require the organisation of VLIW instructions in a specific manner before being routed to the pipelines. The present invention also dispenses with the extra processing power/circuitry needed in Tremblay. Thus, Tremblay cannot be said to anticipate the present invention, as claims 1 and 22 have now been amended to incorporate the feature that all the pipelines have substantially the same instruction processing capability. Withdrawal of this rejection is respectfully requested.

Claims 1 and 19-22 stand rejected under § 102 on the basis of Murty. Remaining independent claims 1 and 22 have been amended to overcome this rejection, by reciting that the pipelines are flushed in response to a stall signal being generated.

Turning to Murty, it is noted from Figure 4 and the discussion spanning from column 5, lines 46 to column 6, line 12, that the processor disclosed therein operates in the following way: (1) initially, the multiple pipelines (two have been referred to for the sake of simplicity in this example) operate synchronously (410); (2) the first pipeline generates a local stall (420) which is registered in the second pipeline in a subsequent cycle (i.e. this pipeline progresses in the meantime causing it to be asynchronous with the first pipeline which "freezes" due to the stall); (3) the information in the progressed stage of the second pipeline is stored in a buffer (430); (4) the first and second pipelines are both then flushed and the information from the buffer (saved in step (3)) is retrieved and loaded into the first stages of both the pipelines (440); and (5) after the stall condition has been released, synchronisation between the pipelines is achieved by staggering the second pipeline by the same number of cycles that it was ahead by in step (2) with respect to the first pipeline.

The present invention differs from the disclosure in Murty since the pipelines are not flushed in response to a stall signal being generated. This offers the advantage that extra processing power and time are not used in generating the flush signal, flushing the pipelines, retrieving the information saved in the buffer and reloading it in the pipelines, as would be the case in Murty. Thus, Murty cannot be said to anticipate the present invention. Claim 1 has now been amended to also include the feature of claim 12, namely, that the

pipelines are not flushed in response to a stall signal being generated. Withdrawal of this rejection is also requested.

For the foregoing reasons, applicants believe that this case is in condition for allowance, which is respectfully requested. The examiner should call applicants' attorney if an interview would expedite prosecution.

Respectfully submitted,

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